REMARKS

I. General

Claims 1-23 were pending in the present application, and all of the pending claims are rejected in the current Final Office Action (mailed February 28, 2005). The outstanding issues raised in the current Office Action are:

- Claims 1-4, 10-14, and 19-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,930,819 issued to Hetherington et al (hereinafter "*Hetherington*"); and

- Claims 1-3, 5-9, 11-12, and 14-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,711,654 issued to Rangan (hereinafter "*Rangan*") in view of U.S. Patent No. 5,226,133 issued to Taylor et al. (hereinafter "*Taylor*").

In response, Applicant respectfully traverses the outstanding claim rejections, and requests reconsideration and withdrawal thereof in light of the amendments and remarks presented herein.

II. Amendments

Claim 1 is amended and claims 11-20 and 22-23 are deleted without prejudice. More specifically claim 1 is amended to include the element previously presented in claim 22, which depended from claim 1. Therefore, claim 22 is deleted. Claims 11-20 and 23 are deleted without prejudice. Applicant respectfully requests entry of these amendments as they raise no new issues and place the present application in condition for allowance or better condition for appeal.

III. Rejections Under 35 U.S.C. § 102

Claims 1-4, 10-14, and 19-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Hetherington*. Claims 11-14, 19-20, and 22-23 are deleted without prejudice herein, and therefore this rejection of those claims is moot. As to claims 1-4, 10, and 21, Applicant respectfully traverses these rejections as provided further below.

To anticipate a claim under 35 U.S.C. § 102, a single reference must teach every element of the claim, *see* M.P.E.P. § 2131. Applicant respectfully submits that *Hetherington* does not teach each and every element of claims 1-4, 10, and 21.

Independent Claim 1

Hetherington fails to teach all elements of independent claim 1, as amended herein. Claim 1, as amended herein, recites in part "circuitry operable to determine a bank conflict for pending access requests for said cache memory structure, wherein said circuitry is operable to determine said bank conflict using bits of virtual addresses to be accessed by said pending access requests" (emphasis added).

Hetherington does not teach using bits of virtual addresses for determining bank conflicts, wherein the bits of the virtual addresses include bits that correspond to bits of physical addresses to be accessed by a pending access request. The Final Office Action asserts, at page 8 thereof, that *Hetherington* "teaches using virtual addresses (instead of physical addresses) to access the L2 cache", citing column 13, lines 33-35 of *Hetherington*. *Hetherington* teaches a system in which physical addresses (PAs) are used for determining bank conflicts. Column 13, lines 33-35 of *Hetherington* provides: "If the level 2 cache were virtually addressed, the PA fields would be equivalently substituted by virtual address bits."

However, *Hetherington* does not teach using such virtual address bits for determining bank conflicts. Rather, *Hetherington* specifically teaches that when virtual addresses are used, the virtual address is received at the cache and first translated to a physical address and the physical address is used for determining bank conflicts. For instance, as shown in FIGURE 5, virtual addresses (VAs) are received into the micro-TLBs 501 and translated into physical addresses, which are supplied to MSW 502 for determining bank conflicts. As *Hetherington* explains at column 10, lines 48-62:

> In a particular example, IEU 208 includes two memory pipes M0 and M1 generating effective virtual addresses (indicated by M0 VA and M1 VA in FIG. 5) for integer and floating point load and store operations. IEU 208 also includes two arithmetic logic units (ALU0 and ALU1) generating virtual addresses (indicated by ALU0 VA and ALU1 VA) dedicated for floating point loads and stores. Virtual to physical address translation occurs in a conventional manner through micro translation lookaside buffers (μTLBs) 501 that are hardware controlled subsets of a main translation lookaside buffer

> (TLB) (not shown) TLBs store the most-recently used virtual:physical address pairs to speed up memory access by reducing the time required to translate virtual addresses to physical addresses needed to address memory and cache. (Emphasis added).

As FIGURE 5 shows, the virtual addresses are translated by TLBs 501, and the resulting physical addresses are supplied to MSW 502 for determining bank conflicts. The picker 606 of FIGURE 6 selects valid entries from MSW 502 to launch each clock cycle, see Col. 14, lines 22-42. Thus, because MSW 502 includes physical addresses, picker 606 does not determine a bank conflict based on virtual addresses.

Further, claim 1, as amended herein, recites "wherein said circuitry is operable to determine said bank conflict using bits of virtual addresses to be accessed by said pending access requests, and wherein said bits of virtual addresses include bits that correspond to bits of physical addresses to be accessed by said pending access requests" (emphasis added). *Hetherington* fails to teach this element of claim 1. Column 13, lines 33-35 of *Hetherington* provides: "If the level 2 cache were virtually addressed, the PA fields would be equivalently substituted by virtual address bits." To the extent that this portion of *Hetherington* teaches that its cache may be virtually addressed, rather than physically addressed, *Hetherington* provides no teaching that bits of the virtual addresses include bits that correspond to bits of physical addresses. Indeed, if the cache is entirely virtually addressed, there would appear to be no such physical address of which bits could be included in the virtual address. In any case, *Hetherington* provides no teaching of this element of claim 1.

In view of the above, the § 102 rejection of claim 1 over *Hetherington* should be withdrawn.

Dependent Claims

In view of the above, Applicant respectfully submits that independent claim 1 is not anticipated under 35 U.S.C. § 102 over *Hetherington*. Further, each of dependent claims 2-4, 10, and 21 depend either directly or indirectly from independent claim 1, and thus inherit all limitations of independent claim 1. It is respectfully submitted that dependent claims 2-4, 10, and 21 are allowable not only because of their dependency from independent claim 1 for the reasons discussed above, but also in view of their novel claim features (which both narrow the scope of the particular claims and compel a broader interpretation of claim 1).

IV. Rejection under 35 U.S.C. § 103(a)

Claims 1-3, 5-9, 11-12, and 14-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Rangan* in view of *Taylor*. Claims 11-12, and 14-20 are deleted without prejudice herein, and therefore this rejection of those claims is moot. As to claims 1-3 and 5-9, Applicant respectfully traverses these rejections as provided further below.

To establish a prima facie case of obviousness, three basic criteria must be met. *See* M.P.E.P. § 2143. First, there must be some suggestion or motivation, either in the applied references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the applied references must teach or suggest all the claim limitations. Without conceding any other criteria, Applicant respectfully asserts that the applied combination of *Rangan* and *Taylor* does not teach or suggest all the claim limitations.

Independent Claim 1

Independent claim 1 is amended herein to include the element of dependent claim 22. Because claim 22 is not rejected under 35 U.S.C. § 103(a) as being unpatentable over *Rangan* in view of *Taylor*, Applicant respectfully submits that claim 1, as amended, should not be so rejected.

Dependent Claims

Further, each of dependent claims 2-3 and 5-9 depend either directly or indirectly from independent claim 1, and thus inherit all limitations of independent claim 1. It is respectfully submitted that dependent claims 2-3 and 5-9 are allowable not only because of their dependency from independent claim 1 for the reasons discussed above, but also in view of their novel claim features (which both narrow the scope of the particular claims and compel a broader interpretation of claim 1).

V. Conclusion

In view of the above, Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 10971529-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Label No. EV 482708457US in an envelope addressed to: M/S After Final, Commissioner for Patents, Alexandria, VA 22313.

Date of Deposit: April 26, 2005

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